REMARKS

In accordance with the foregoing, the claims have been amended. Claims 10 and 13 have been previously cancelled. Claims 1-5, 9 , 11 and 14 have been amended. Claim 16 is new. Claims 1-9, 11, 12 and 14-16 are pending and under consideration. The rejections are respectfully traversed.

Rejections under U.S.C. § 102

Claims 1-6 and 15 stand rejected under 35 U.S.C. § 102(b) as anticipated by Miura. Miura discusses a CAD system for determining the best placement of components based on a center of gravity method and the routing paths of connections between the components on a printed circuit board. The method of the system is iterative in that a user is presented with a drawing of a printed circuit board; defines a component and its connections to other components on the printed circuit board; then allows the system to define the placement of the component and best path for the connectors, if one can be found; displays the updated drawing of the printed circuit board; the steps are repeated for the next component. Miura shows how to place circuit components on a circuit board.

The present claims discuss a method to improve visibility of connections between logical drawing sheets. This is accomplished by showing on a display, the drawing sheets as miniaturized versions and showing the interconnection of the sheets on the display. (See application Fig. 15)

Claim 1 has been amended to recite in part “a means for creating an inter-drawing diagram file which describes respective positions of said plurality of drawing sheets on one screen and attributes of said plurality of drawing sheets.” Support for the amendment found in the disclosure at paragraph 0021. Miura Fig. 5D does not teach or suggest an inter-drawing diagram file, nor means for creating one, nor one that interrelates drawing sheets. Miura Fig. 5D discusses “[r]outing pattern information is composed of: an identifier given to a connector; a net name given to the connector; an identifier of a surface on which the connector is routed; a number of constituting points of the connector; and coordinates of the constituting points.” Column 13 lines 15-19.

Amended claim 1 further recites in part ”inter-drawing indication means for indicating, on said screen, said plurality of drawing sheets according to the description in said inter-drawing diagram file by miniaturized the size of each of said plurality of drawing sheets; and net drawing means for drawing nets among said plurality of drawing sheets miniaturized and indicated on

said screen, said nets indicating connection relations among a plurality of symbols contained in different ones of said plurality of drawing sheets."

Miura Fig. 8 does not teach or suggest a plurality of "drawing sheets miniaturized and indicated on said screen, said nets indicating connection relations among a plurality of symbols contained in different ones of said plurality of drawing sheets."

Column 14 lines 34-45 of Miura in discussing Fig. 8 states:

> An example of high resolution display 2 is shown in Fig. 8. The outline a large L-like figure represents a circuit board. A rectangular on whose opposing two sides are attached small squares represents an IC, each of the small squares representing a terminal. A big square having terminals on its four sides represents chip surface packaging component of a flat package. A small rectangle which is divided by two lines in itself represents resistance, and a small circle represents a via. Thick broken lines, horizontal lines and vertical lines represent connectors. Actual size proportion of them all is represented accurately by the design information in storage device 1.

As can be seen from the above discussion, Fig. 8 shows an outline of an L-like figure representing a circuit board its components and how their connectors are laid out. It does not show a plurality of miniaturized drawing sheets. Further, the components and connectors within the circuit board are actual size proportions and therefore are further not miniaturized.

Miura Fig. 11A does not show miniaturized drawing sheets connected by nets. What is in fact shown in Figs. 11A, B and C is the conceptual steps of the placement of a components on a printed circuit board. The dotted lines of the reference showing connectors paths that must be set up in the printed circuit board when the method is complete, as shown in Fig 11C.

It is respectfully submitted for the reasons stated above, that claim 1 and any claims that depend therefrom are patently distinguishable over Miura.

As regards claim 2, Examiner cites Miura Fig. 3 S4008 as disclosing the limitation of the second clause of claim 2. What is discussed is "when some components cannot be placed on the circuit board (Step 4004), the designer corrects the circuit board layout by interactive edit (Step 4008). If this correction turns out a success, processing ends (Step 4009). If this is not the case, the designer resets shape of the circuit board and size of each side of it (Step 4001)." Miura does not teach or suggest "inter-drawing diagram editing means for implementing editing works on each of said plurality of drawing sheets when said plurality of drawing sheets are indicated on said screen." It is respectfully submitted for the reasons stated above, that claim 2 and any claims that depend therefrom are patently distinguishable over Miura.

As regards claims 3 and 4, the placement success step 4004 of Miura Fig. 3 is not the "said inter-drawing diagram editing means, further, modifies the position of each drawing sheet on said screen." of claim 3. Likewise, step "route connectors between terminals" step 4005 of Miura Fig. 3 is not the modifying "the position of each drawing sheet on an said screen" of claim 4. Each of these is a step of a process not shown on one screen.

It is respectfully submitted for the reasons stated above, that claims 3 and 4 are patently distinguishable over Miura.

As regards claims 5 and 6, the "constituting points" of Miura Fig. 5D are not analogous to connectors of the claims. Fig. 5D shows them to be points where the foil of a connector changes direction. It is respectfully submitted for the reasons stated above, that claims 5 and 6 are patently distinguishable over Miura.

As regards claim 15, the "plurality of miniaturized drawing sheets are drawn in a shape of a block diagram" of the claim is not analogous to a display of "function block information describes which function block includes a placement candidate component and which area on a circuit board is assigned to each function block." Column 34 lines 52-54 of Miura. It is respectfully submitted for the reasons stated above, that claim 15 is patently distinguishable over Miura.

Claim 14 stands rejected under 35 U.S.C. § 102(b) as anticipated by Otaguro. Otaguro discusses dividing an area of a chip into a plurality of regions so as to estimate a wire capacity based on connection information of instances disposed in the respective regions. Reference marks r1 and r2 of Fig. 15 of Otaguro as discussed at column 12 lines 2 and 3 represent the regions formed by dividing a chip. Otaguro does not teach or suggest a "hierarchical design of a logic circuit comprises a plurality of symbols." Otaguro, therefore does not teach or suggest the "logic drawing entry apparatus for drawing a plurality of drawing sheets for hierarchical design of a logic circuit, comprising: judging means to determine if a particular level of hierarchical design of a logic circuit comprises a plurality of symbols, each of which belongs to the same level as said particular level; drawing means for drawing a plurality of drawing sheets by dividing said plurality of symbols into individual symbols so that each of said drawing sheets comprises at least one of said symbols, if said judging means determines that said particular level of hierarchical design of a logic circuit comprises a plurality of symbols, each of which belongs to the same level as said particular level; and a net drawing means for drawing nets for each of said symbols," of amended claim 14. Support for the amendment found in the specification at paragraphs 0072-0073.

Further, Fig. 16 of Otaguro is a "flowchart showing the procedure of the wire load estimating method", it has neither "a net drawing means" or "drawing means for drawing a plurality of drawing sheets" as no drawing means is disclosed.

It is respectfully submitted for the reasons stated above, that amended claim 14 is patently distinguishable over Miura.

Rejection under U.S.C. § 103

Claims 7 and 8 stand rejected under 35 U.S.C. § 103(a) as obvious over Miura in view of Merchant. Merchant is a system for automatically identifying configuration memory cell addresses in a schematic hierarchy. The memory cells of Merchant are not analogous to the drawing sheets of the present invention and therefore there would be no suggestion to combine the references. Agrawal or Eldridge

Therefore, the combination of Miura and Merchant fail to establish a prima facie case of obviousness over the present invention.

Claims 9, 11 and 12 stand rejected under 35 U.S.C. § 103(a) as obvious over Agrawal in view of Eldridge. Claim 9 has been amended to further clarify and distinguish the claim from Agrawal. Claim 9 further recites a "judging means for judging whether or not a symbol exists at said position selected." Support for the amendment found in paragraph 0056 of the disclosure. Agrawal not disclosing a "symbol moving means for moving said selected symbols to said position if there is no symbol at said selected position."

Therefore, it is respectfully submitted that Agrawal or Eldridge taken alone or in combination fails to disclose, teach or suggest the limitations of claim 9 or the claims dependent therefrom.

NEW CLAIM

Claim 16 is new. Support for claim 16 can be found in paragraph 0021 of the disclosure. The prior art not disclosing a "method of displaying a relationship between a plurality of drawing sheets for computer aided design of logic circuits, the method comprising: displaying the plurality of drawing sheets according to the description in a inter-drawing diagram file, each drawing sheet of the plurality of drawing sheets reduced in size to allow the displayed plurality of drawing sheets to exist on a single screen; and drawing nets among the plurality of reduce drawing sheets, the nets indicating the relative relationship among a plurality of symbols contained in each drawing sheet of the plurality of drawing sheets."

SUMMARY

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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